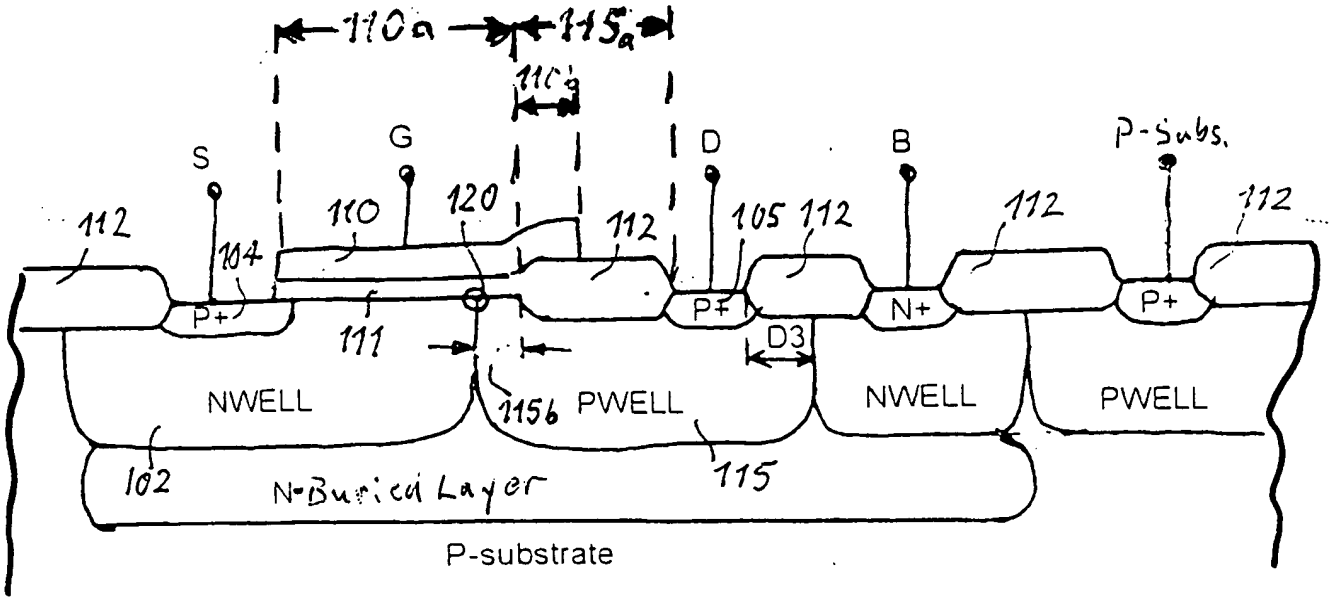


FIG. 1 (PRIOR ART)

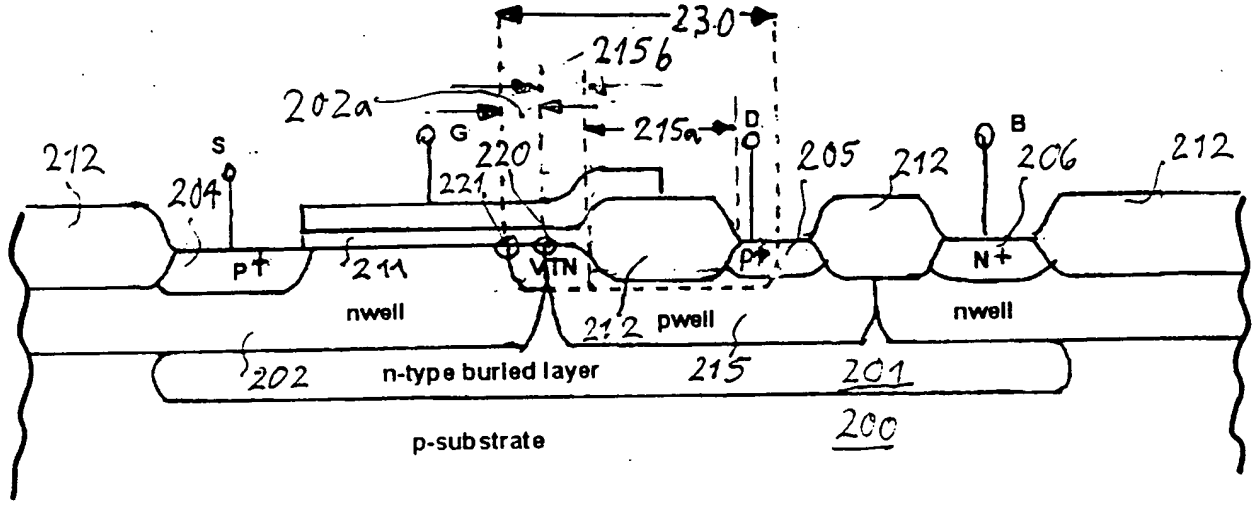
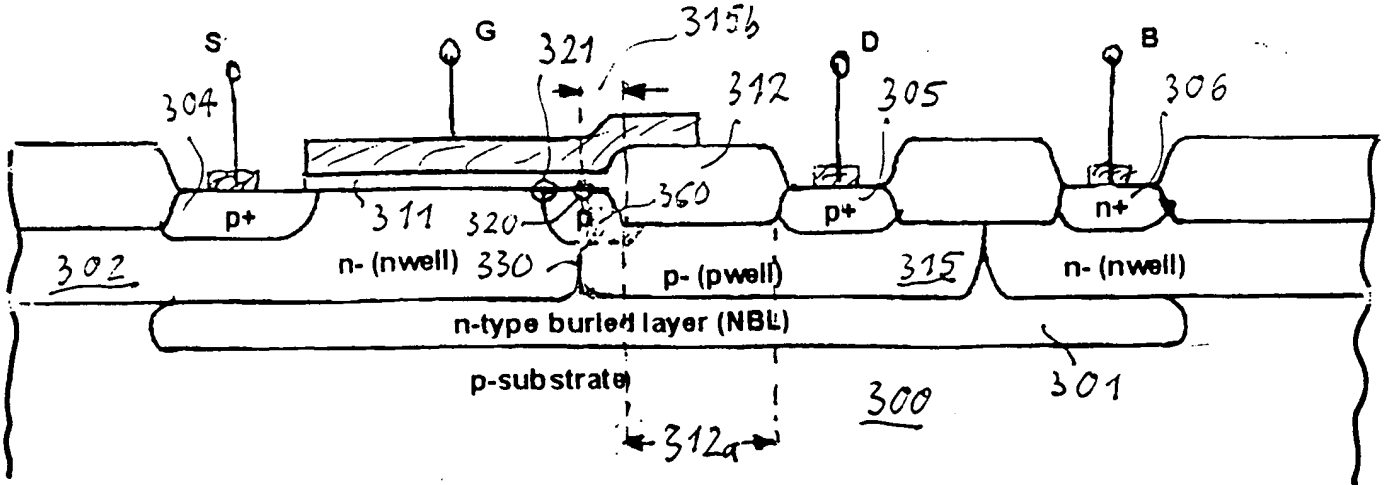


FIG. 2



BEST AVAILABLE COPY

FIG. 3

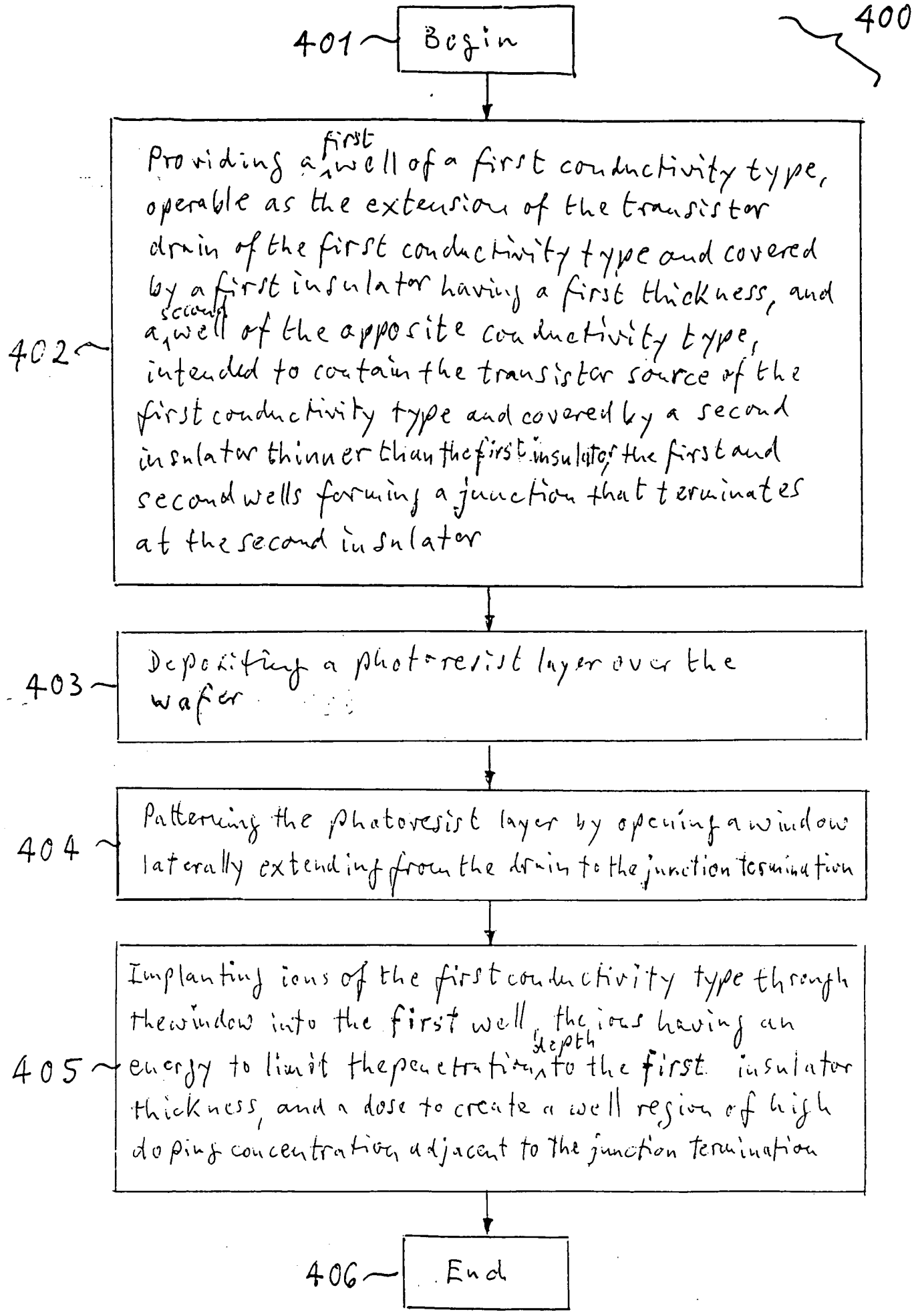

400
401
Begin
402
Providing a first well of a first conductivity type, operable as the extension of the transistor drain of the first conductivity type and covered by a first insulator having a first thickness, and a second well of the apposite conductivity type, intended to contain the transistor source of the first conductivity type and covered by a second insulator thinner than the first insulator, the first and second wells forming a junction that terminates at the second insulator
403
Depositing a photoresist layer over the wafer
404
Patterning the photoresist layer by opening a window laterally extending from the drain to the junction termination
405
Implanting ions of the first conductivity type through the window into the first well, the ions having an energy to limit the penetration depth to the first insulator thickness, and a dose to create a well region of high doping concentration adjacent to the junction termination
406
End

FIG. 4

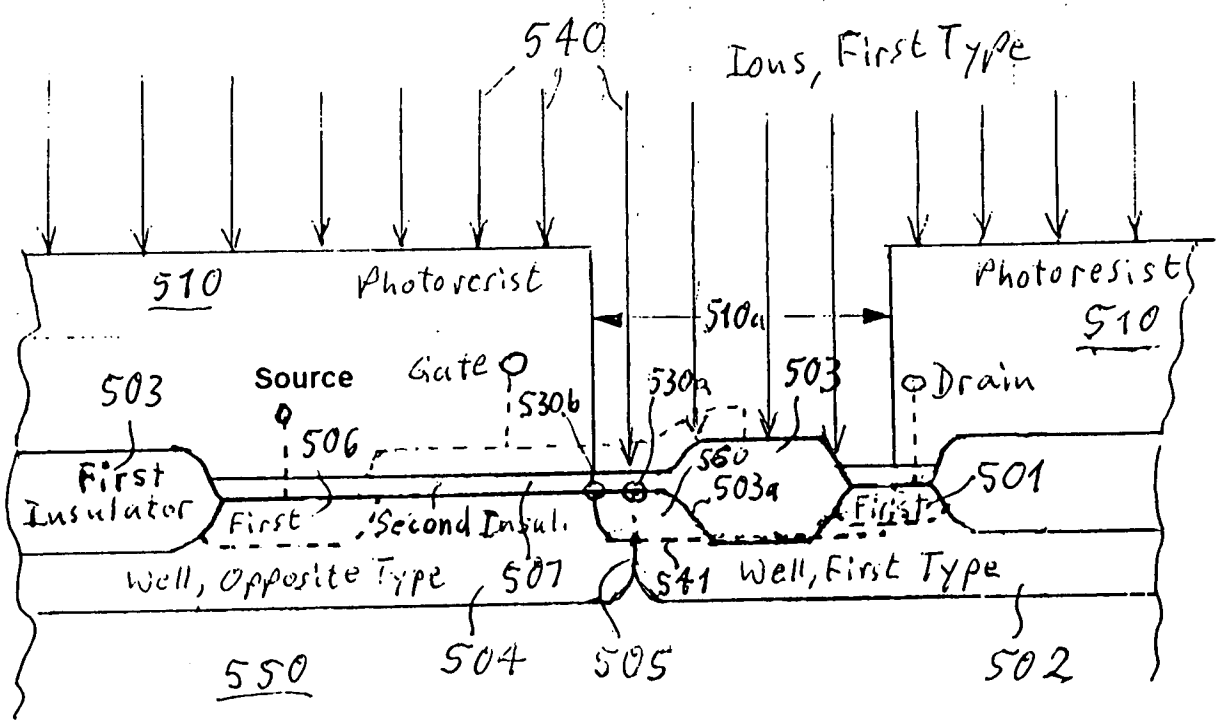
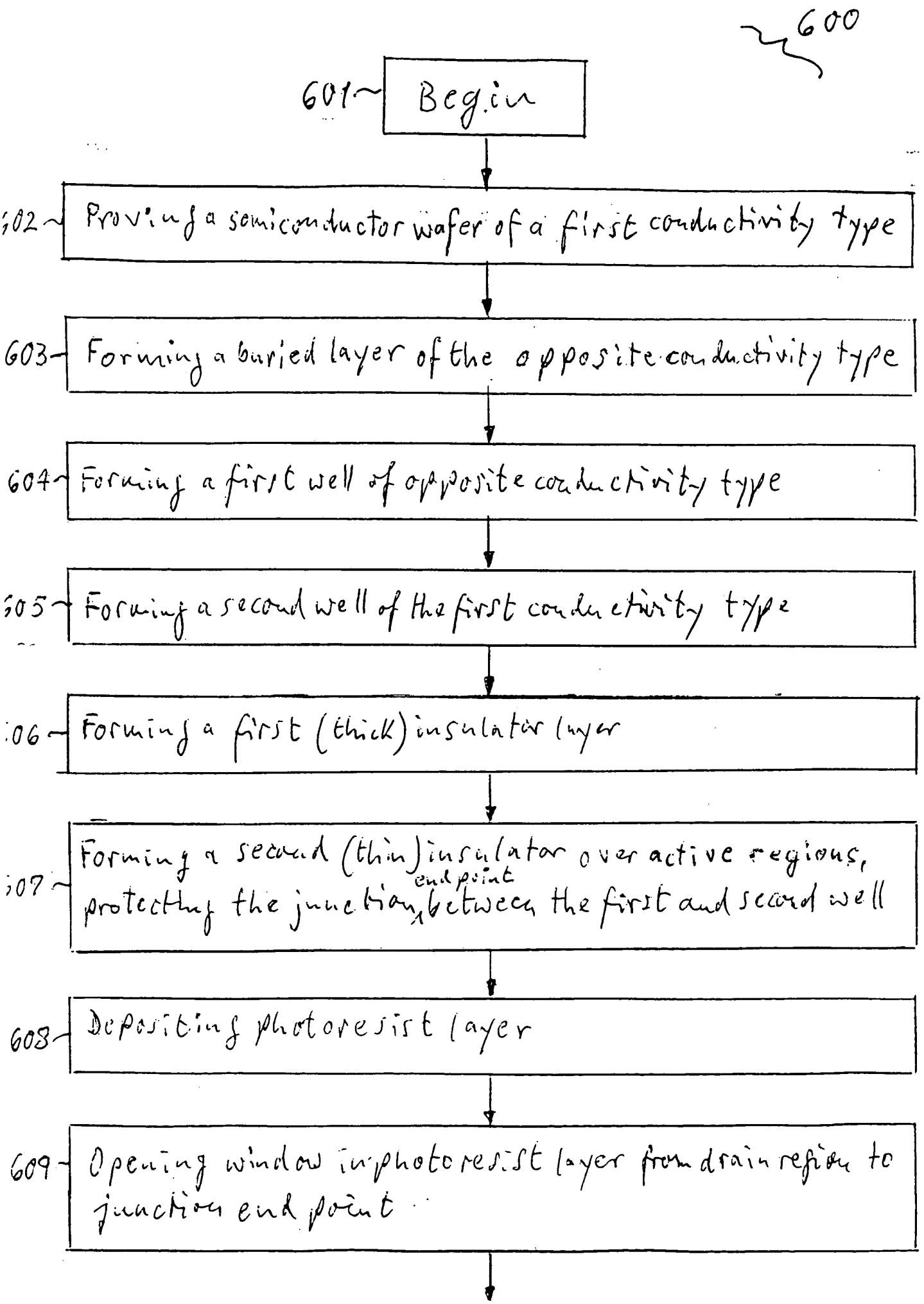

540
Ions, First Type
510
Photoresist
510a
Photoresist
510
503
Source
Gate
530b
530a
503
Drain
506
560
First Insulator
First
Second Insul.
503a
First
501
Well, Opposite Type
507
541
Well, First Type
550
504
505
502

FIG. 5


600
601
Begin
602
Proving a semiconductor wafer of a first conductivity type
603
Forming a buried layer of the opposite conductivity type
604
Forming a first well of opposite conductivity type
605
Forming a second well of the first conductivity type
606
Forming a first (thick) insulator layer
607
Forming a second (thin) insulator over active regions, protecting the junction endpoint between the first and second well
608
Depositing photoresist layer
609
Opening window in photoresist layer from drain region to junction end point

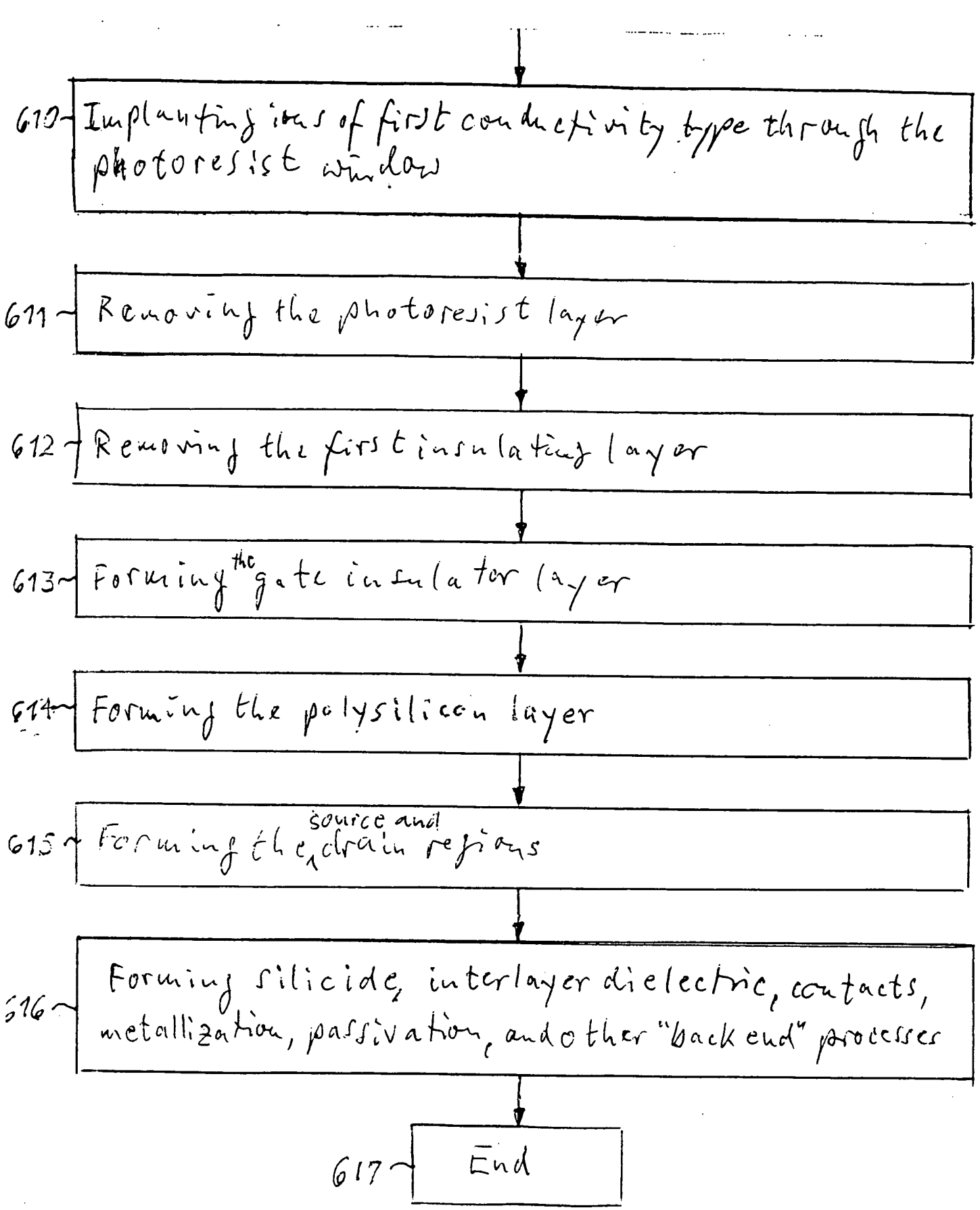

610
Implanting ions of first conductivity type through the photoresist window
611
Removing the photoresist layer
612
Removing the first insulating layer
613
Forming the gate insulator layer
614
Forming the polysilicon layer
615
Forming the source and drain regions
616
Forming silicide, interlayer dielectric, contacts, metallization, passivation, and other "back end" processes
617
End

FIG. 6

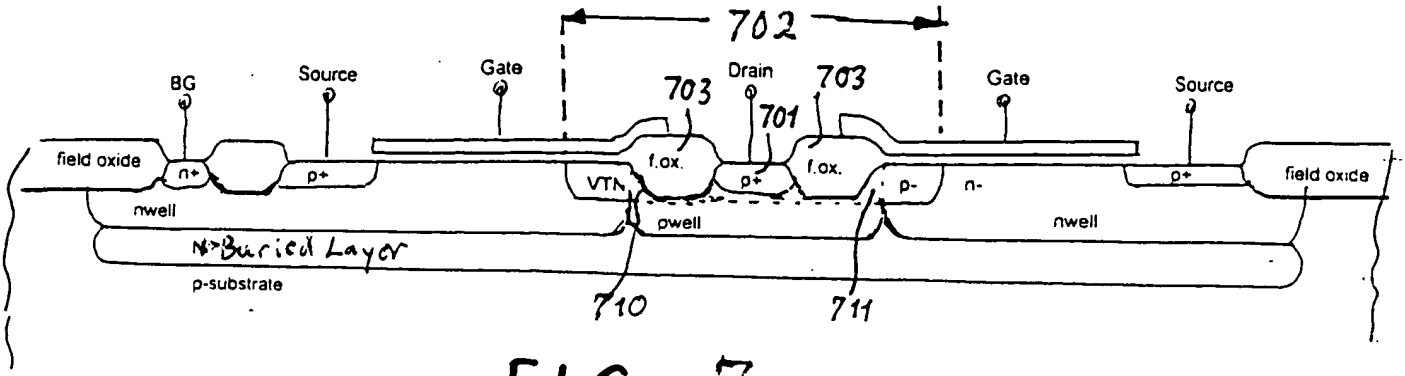

702
BG
Source
Gate
Drain
703
701
703
Gate
Source
field oxide
n+
p+
VTN
f.ox.
p+
f.ox.
p-
n-
p+
field oxide
nwell
pwell
nwell
N+Buried Layer
p-substrate
710
711

FIG. 7

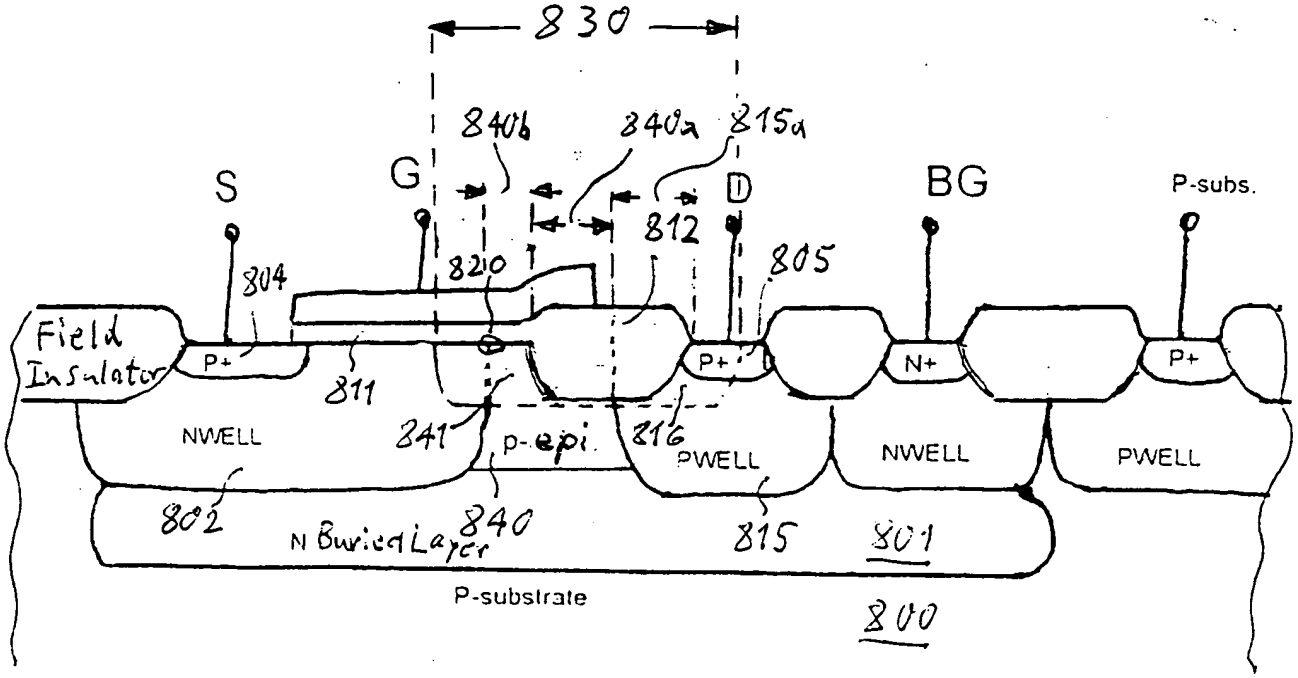

830
840b
840a
815a
S
G
D
BG
P-subs.
812
804
820
805
Field Insulator
P+
811
P+
N+
P+
841
816
NWELL
p-epi
PWELL
NWELL
PWELL
802
840
815
801
N Buried Layer
P-substrate
800

FIG. 8

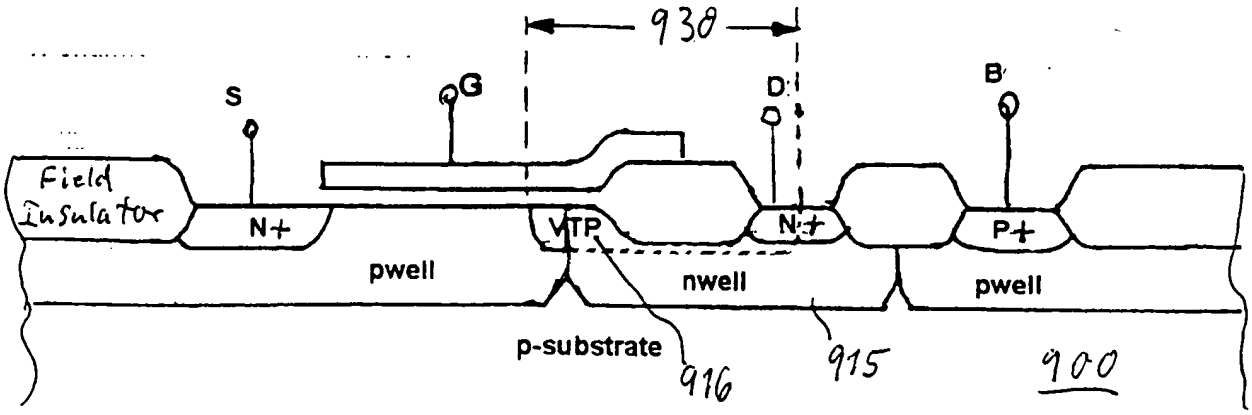

930
S
G
D
B
Field Insulator
N+
VTP
N+
P+
pwell
nwell
pwell
p-substrate
916
915
900

FIG. 9

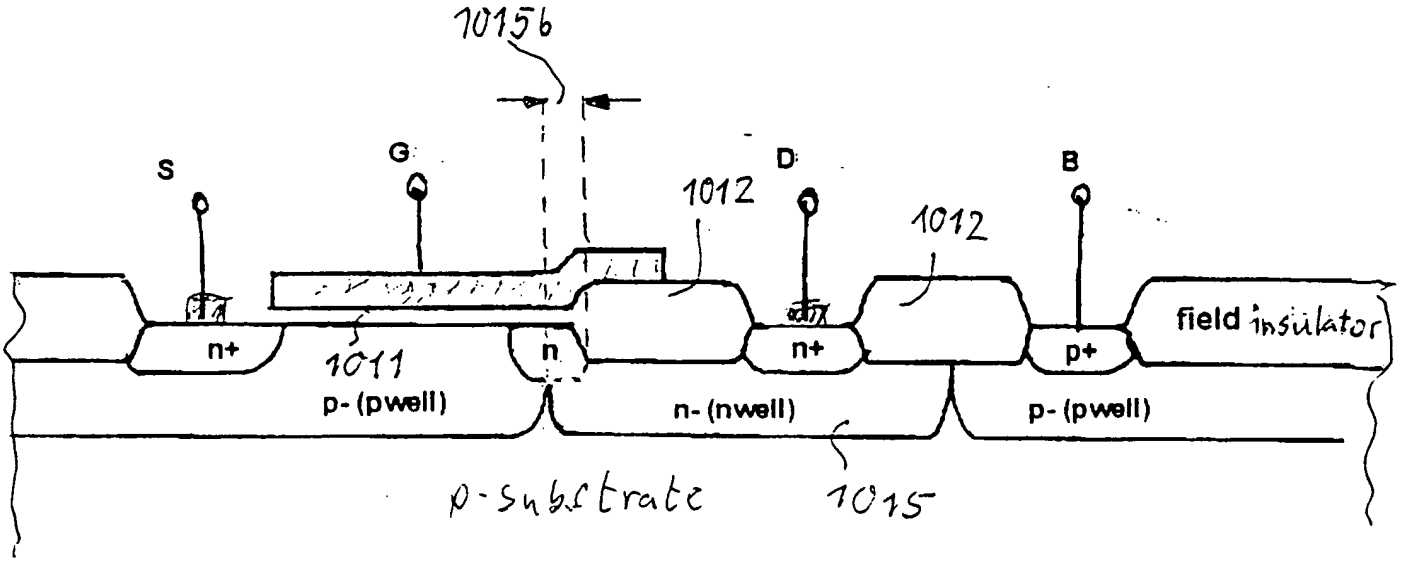

10156
S
G
D
B
1012
1012
n+
1011
p- (pwell)
n
n+
p+
field insulator
n- (nwell)
p- (pwell)
p-substrate
1015

FIG. 10

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☑ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☑ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.